Remarks

The Final Office Action dated April 17, 2008 lists the following rejections: claims 1-3 and 6 stand rejected under U.S.C. § 102(b) over the Wieczorek reference (U.S. Patent No. 6,274,894); claims 4-5 stand rejected under 35 U.S.C. § 103(a) over the Wieczorek reference in view of the Chau reference (U.S. Patent No. 5,710,450); claims 7-11 stand rejected under U.S.C. § 103(a) over the Chau reference in view of the Andideh reference (U.S. Patent No. 6,121,100) and further in view of the Wieczorek reference.

Applicant submits that the rejections are erroneous and based on a misinterpretation of the claims. In particular, the rejections are based an attempt to find correspondence between the applied references and Applicant's Fig. 7, rather than the features recited in the claims. In so doing, the Examiner has failed to address all the elements of the claims, and furthermore has incorrectly interpreted elements from the drawings.

The § 102(b) rejection is erroneous because the Wieczorek reference fails to disclose aspects of the claimed invention related to a second semiconductor material disposed below the level of a gate insulating layer and that extends substantially as far as a gate electrode sidewall. Wieczorek's semiconductor portions 56 do not extend as far as a gate electrode sidewall, and in fact are prevented from doing so. Wieczorek's Figs. 7 through 9 (Fig. 9 reproduced below) and corresponding description clearly indicate that the process for forming trenches 52 self-aligns the trenches to the outside edges of the dielectric sidewalls 50, which are outside of the sidewalls of gate conductor 44. The trenches 52 are then filled with a layer 54 and then with semiconductor portions 56. The extension of portions 56 is limited by the extension of trenches 52, which is prevented from reaching the gate sidewalls.

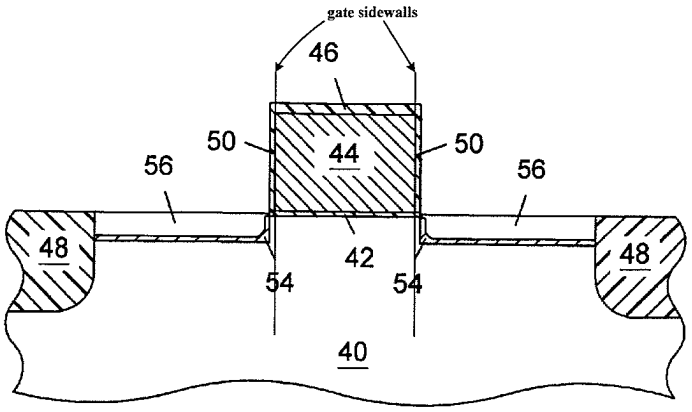

Fig. 9

Therefore, Wieczorek's semiconductor portions 56 cannot be said to correspond to the portions of second semiconductor material recited in Applicant's claims. Accordingly, the § 102(b) rejection of claims 1-3 and 6 is improper and Applicant requests that it be withdrawn.

As best understood by Applicant, the Final Office Action responds to Applicant's arguments by attempting to interpret the claims in light of Applicant's Fig. 7 (reproduced below) and in a manner that reads on the transistor of Wieczorek. In so doing, the Final Office Action tacitly admits that the portions 56 of Wieczorek do not extend all the way to the gate electrode sidewall. Instead it is argued that the claim language "extends ... substantially as far as" encompasses Applicant's Fig. 7 and Wieczorek. Applicant submits that the Final Office Action mischaracterizes Applicant's teachings and misinterprets the claims. For example, the Final Office Action states that portions 8 and 9 shown in Applicant's Fig. 7 do not extend all the way to the sidewalls of gate electrode 1, and therefore the portions 56 of Wieczorek need not extend all the way to the gate sidewalls to anticipate the claims. Applicant submits that portions 6 and 7 in Fig. 7 are shown to extend as far as the limit line of the gate sidewall, and that the extension of portions 8 and 9 in Fig. 7 is not relevant. The claims clearly recite that the portions of the second material extend at least partially between the substrate and a spacer. As seen in Fig. 7, portions 6 and 7 are shown to extend between the substrate 100 and the spacer 30, whereas portions 8 and 9 do not. Claim 1 also recites that the portions of the second material are disposed below the level of a gate insulating layer. As seen in Fig. 7, portions 6 and 7 are disposed below the gate insulating layer 2, whereas portions 8 and 9 are not.

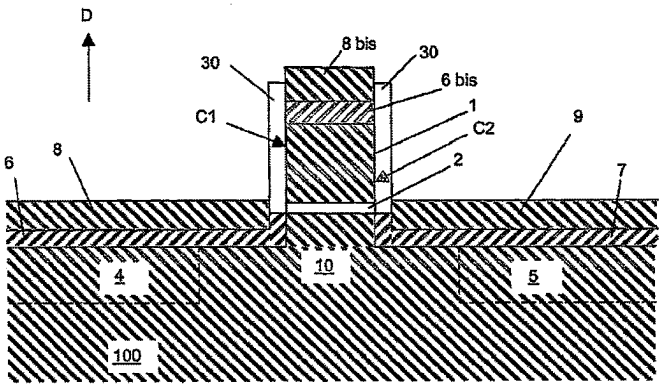

FIG. 7

Applicant further points to the teachings in the specification, which clearly state, for example, "[e]ach portion 6 or 7 is extended substantially as are as a location coming in line ... with the side C1 or C2 of the electrode 1" (*see* paragraph 0025). Applicant therefore submits that there is no basis to interpret the phrase "extends ... substantially as far as" in a manner that would read on the Wieczorek reference.

Regarding the assertion in the Final Office Action that "It is entirely possible that the trenches could be aligned to the inner sidewalls of dielectrics 50 which would mean that they would extend directly to the gate conductor," Wieczorek explicitly teaches that the process for forming trenches 52 self-aligns the trenches to the outside edges of the dielectric sidewalls 50 as discussed above. Applicant notes that "possible" is an insufficient standard to support a § 102 rejection. *See, e.g.,* M.P.E.P. §§ 2112 and 2131 ("A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.").

For at least the reasons presented above, the § 102(b) rejection of claims 1-3 and 6 is improper and Applicant requests that it be reconsidered and withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 4-5 (based upon the Wieczorek reference) because the cited portions of Wieczorek do not correspond to the claimed invention as discussed above in relation to the § 102(b) rejection of claim 1. In at least this regard, the § 103(a) rejection of claims 4-5 is improper in that these claims depend from claim 1. Therefore, Applicant requests that the § 103(a) rejection of claims 4-5 be withdrawn.

Applicant further traverses the § 103(a) rejection of claim 5 because the cited portions of the Chau reference do not correspond to aspects of the claimed invention directed to each encapsulation portion extending between the spacer and the portion of second semiconductor material above which said encapsulation portions is deposited. The Office Action erroneously asserts that Chau's second semiconductor material 420 corresponds to the claimed encapsulation portions. However, as is clearly shown by Chau in Figure 4, Chau's second semiconductor material 420 does not extend between semiconductor material 314 and sidewall spacer 318. Thus, Chau's second semiconductor material 420 does not correspond to the encapsulation portions of the claimed invention. Again, the only basis for disagreement stated in the Final Office Action relies on the same misinterpretation of Applicant's claims and Fig. 7 as noted above. Applicant further notes that Applicant's Fig. 1 shows encapsulation portions 8 and 9 that extend under spacers 3 and substantially in line with the side C1 or C2 of the electrode 1 as is commensurate with the scope of claim 5. Accordingly, the § 103(a) rejection of claim 5 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 7-10 because the cited portions of the Chau and Andideh references do not correspond to various aspects of the claimed invention as was discussed in detail in the Response of January 7, 2008, hereby incorporated by reference in its entirety. Once again, the only basis for disagreement stated in the Final Office Action relies on the same misinterpretation of Applicant's claims and Fig. 7 as discussed above in relation to the § 102(b) rejection of claim 1. Accordingly, Applicant submits that the § 103(a) rejection of claims 7-10 is improper, and requests that it be reconsidered and withdrawn.

Applicant further submits that the § 103(a) rejection of claims 7-10 is erroneous because none of the cited references teach or suggest heating the second material so that the portions of second material contain electrical carriers with concentrations lower than that of the deeper source and drain regions. The Final Office Action relies on the Andideh reference for allegedly disclosing the claimed heating step, but fails to address the resulting electrical carrier concentration. Rather than disclosing that heating results in a second material carrier concentration lower than that of the deeper region, Andideh's Fig. 3h and corresponding discussion disclose that carriers diffuse from the region 318

into the area 312 to extend the deeper region 310. Carrier diffusion occurs from areas of higher concentration to areas of lower concentration. As such, Andideh's region 310 cannot end up with a higher concentration than the region 318, and therefore cannot be read on Applicant's claims. Accordingly, the § 103(a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 7-10 because the cited portions of the Wieczorek reference do not correspond to claimed aspects directed to heating the portions of second semiconductor material to a temperature that is between the melting points of the first and second semiconductor materials. The cited portions of Wieczorek simply teach that an anneal is performed. *See, e.g.,* Col. 13:20-45. However, these portions of Wieczorek fail to make any mention of the temperature at which the annealing is performed, much less that it is performed at a temperature that is between the melting points of first and second semiconductor materials as in the claimed invention. Thus, the cited portions of the Wieczorek reference do not correspond to the claimed invention.

In response to Applicant's argument, the Examiner states that "the cited portions of the Wieczorek reference implicitly anticipates the limitations of claims 7-10." However, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *See* M.P.E.P. § 2112. Inherency may not be established by probabilities or possibilities. As the cited portions of the Wieczorek reference make no mention of the temperature at which the annealing is performed, Applicant submits that the anneal could be performed at a temperature that is less than the melting points of both Wieczorek's first and second semiconductor materials. Thus, the Examiner has failed to establish that the allegedly inherent characteristic necessarily flows from the teachings of Wieczorek (*i.e.*, that Wieczorek implicitly anticipates the limitations of claims 7-10). Accordingly, the § 103(a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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